SHEET INDEˇ

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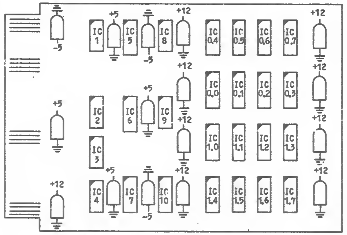
SYMBOL

TERM.MOD.	FUNCT	TERM	LOC
CASIO	I	014	2F0
CEA0I1	I	202	2D0
CEA1I1	I	009	2C0
CEA2I1	I	209	2B0
RASIO	I	003	2E0
RCA0IO	I	007	2H0
RCA1IO	I	205	2G0
RCA2IO	I	006	2G0
RCA3IO	I	203	2G0
RCA4IO	I	201	2F0
RCA5IO	I	002	2F0
RCA6IO	I	206	2F0
RFFIO	I	208	2E0
RWIO	I	001	2H0
WRTD0IO	I	218	2A8
WRTD1IO	I	216	2A9
RDD00	Ø	214	2G9
RDD10	Ø	212	2G9
-5	P	019	3A0
+5	P	011	3D0
+5	P	211	3B0
+12	P	000	3G0
GRD	G	0GD	3C0
GRD	G	004	2F6
GRD	G	005	2F6
GRD	G	008	2F6
GRD	G	2GD	3C0
GRD	G	200	3G0
GRD	G	204	2F6
GRD	G	207	2F6
GRD	G	213	3B0
GRD	G	215	3B0
GRD	G	217	3B0
GRD	G	219	3B0

RECORD OF CHANGES

DWG ISS	PREV FURN	STD	MFR DISC	SEE NOTE

4. INTEGRATED CIRCUIT LOCATION GUIDE:
(COMPONENT SIDE SHOWN)



UNMARKED COMPONENTS ARE FILTER CAPACITORS.

NOTES:

1. UNLESS OTHERWISE SPECIFIED:
RESISTANCE VALUES ARE IN OHMS
CAPACITANCE VALUES ARE IN MICROFARADS
VALUES PRECEDED BY THE SYMBOL + (PLUS) OR - (MINUS) ARE IN VOLTS.

2. POWER AND GROUND TERMINALS FOR INTEGRATED CIRCUITS:

IC CODE	GRD TERM.	-5 TERM.	+5 TERM.	+12 TERM.
28A	16	1	9	8
418P	8		16	
41CD	8		16	
41U	8		16	
KS-21814,L1	7		14	
KS-21827,L14	7		14	

3. BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT PACK ARE AS FOLLOWS:

FUNCTION	TERMINAL
-5	019
+5	011,211
+12	000
GRD	0GD,2GD,004, 005,008,200, 204,207,213, 215,217,219

4. CURRENT DRAINS ASSUMING TIMING SHOWN ON SHEET 5:

SUPPLY	VOLTAGE	CURRENT
VDD	+12V±0.1	70mA
VBB	-5V±0.1	2mA
VCC	+5V±0.1	230mA

DWG ISSUE	DATE ISSUE	DRAWN	APPD
1	3-2-78	NA-TAB TLB	MM JOB MG

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IH

SUPPORTING INFORMATION

CATEGORY	NUMBER
CONNECTOR ON FRAME	947A OR 947C
CIRCUIT PACK INFORMATION DRAWING	
SERIES FOR LATEST CLASS "A" CHANGE	
ACCEPTABLE SERIES	1

SHEET INDEX NOTES

1. ONLY THE LATEST ISSUE, OR ISSUES IF CONCURRENT, ARE SHOWN IN THE INDEX.
2. FOR REISSUES, A CHANGED OR NEW SHEET IS ASSIGNED THE SAME ISSUE NUMBER AS SHEET 1.
3. THE ISSUE NUMBER OF SHEET 1 IS RECOGNIZED AS THE ISSUE NUMBER OF THE WHOLE DRAWING.

NOTICE- NOT FOR USE OR DISCLOSURE OUTSIDE THE BELL SYSTEM EXCEPT UNDER WRITTEN AGREEMENT.

IN98

JL16 CIRCUIT PACK

128K X 2 BIT MEMORY PLANE
CIRCUIT

AT&TCO
STANDARD

DWG SIZE	ISSUE
6S	1

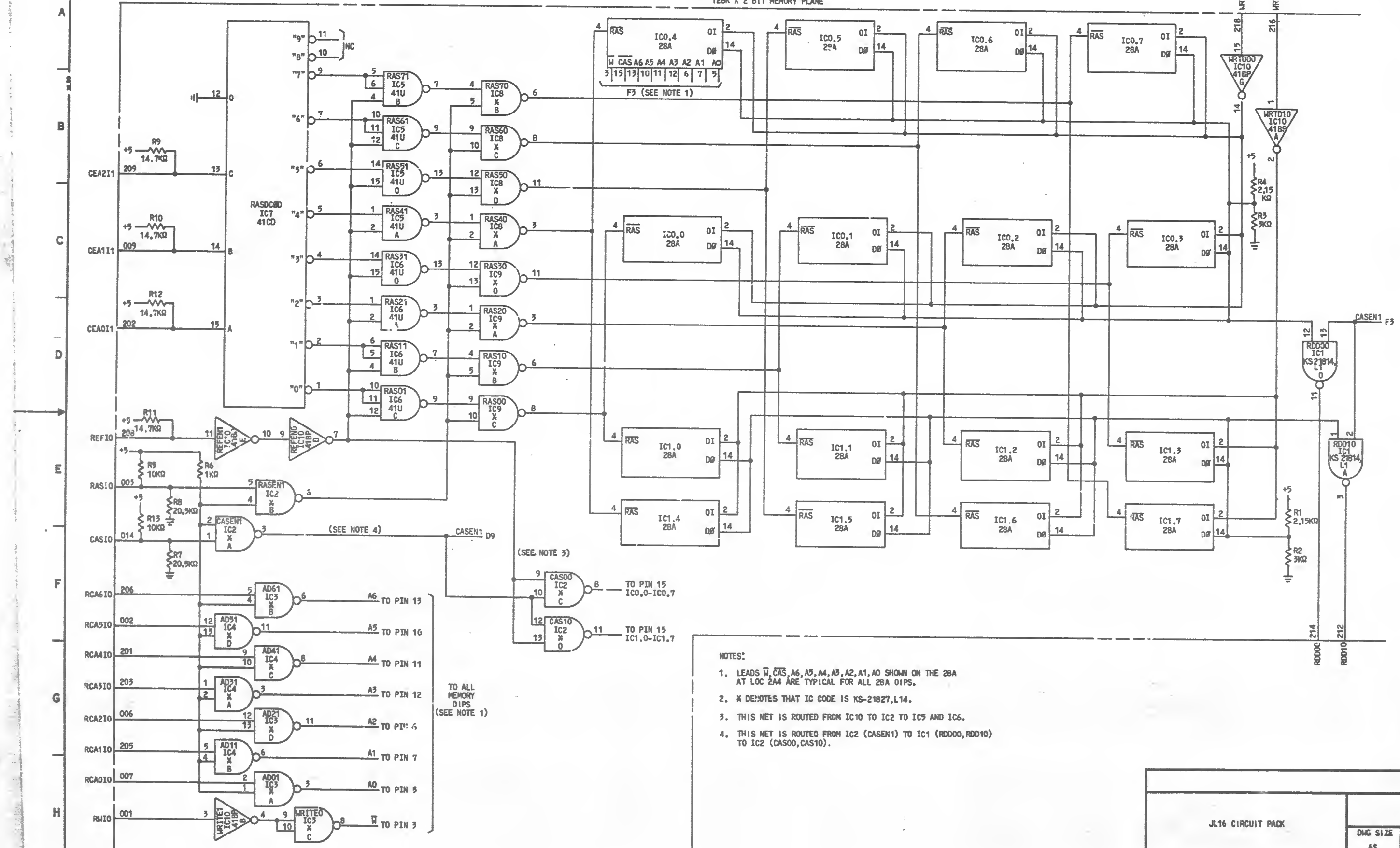
BELL LABORATORIES
CPS-JL16
5 SHEETS

PRINTED IN U.S.A.

8262-070476

PART OF CPS JL16

128K X 2 BIT MEMORY PLANE



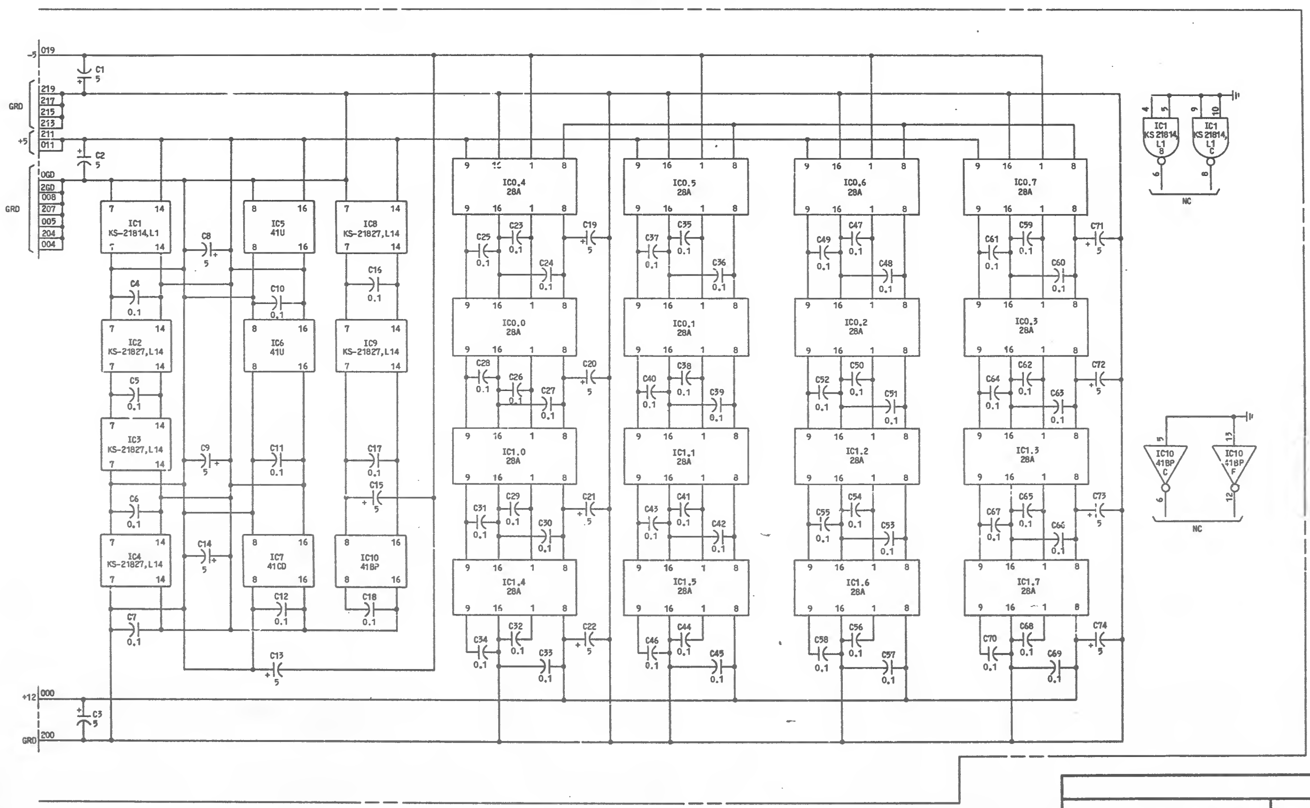
NOTES:

1. LEADS W̄, C̄ĀS̄, A6, A5, A4, A3, A2, A1, A0 SHOWN ON THE 28A AT LOC 2A4 ARE TYPICAL FOR ALL 28A OIPS.
2. X DENOTES THAT IC CODE IS KS-21827,L14.
3. THIS NET IS ROUTED FROM IC10 TO IC2 TO IC5 AND IC6.
4. THIS NET IS ROUTED FROM IC2 (CASEN1) TO IC1 (RDD00,RDD10) TO IC2 (CAS00,CAS10).

JL16 CIRCUIT PACK	DWG SIZE 4S	ISSUE 1
BELL LABORATORIES	CPS-JL16	SHEET 2

PART OF CPS JL16

POWER/GROUND DISTRIBUTION



JL16 CIRCUIT PACK

DWG SIZE 6S

ISSUE 1

BELL LABORATORIES

CPS-JL16

SHEET 3

PART OF CPS JL16

128K X 2 BIT MEMORY PLANE

COMPONENT LIST

INTEGRATED CIRCUITS

LOC	IC1		IC2		IC3		IC4		IC5	
CODE	KS-21814,L1		KS-21827,L14		KS-21827,L14		KS-21827,L14		41U	
ELEM ID	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC
A	RDD10	2E9	CASEN1	2F1	AD01	2H1	AD31	2G1	RAS41	2C2
B			RASEN1	2E1	AD61	2F1	AD11	2H1	RAS71	2B2
C	RDD00	2D9	CAS00	2F3	WRITE0	2H1	AD41	2G1	RAS61	2B2
D			CAS10	2F3	AD21	2G1	AD51	2F1	RAS51	2B2
E										
F										
G										
H										

IC6		IC7		IC8		IC9		IC10		LOC
41U		41CD		KS-21827,L14		KS-21827,L14		41BP		CODE
DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	ELEM ID
RAS21	2D2	RASDC00	2C1	RAS40	2C3	RAS20	2D3	WRTD10	2B8	A
RAS11	2D2			RAS70	2B3	RAS10	2D3	WRITE1	2H1	B
RAS01	2D2			RAS60	2B3	RAS00	2D3			C
RAS31	2C2			RAS50	2B3	RAS30	2C3	REFEN0	2E1	D
								REFEN1	2E1	E
										F
								WRTD00	2A8	G
										H

INTEGRATED CIRCUITS (CONT)

	DESIG	CODE
[8]	IC0.0-IC0.7	28A OR KS-21980,L1
[8]	IC1.0-IC1.7	28A OR KS-21980,L1

CAPACITOR

	DESIG	CODE	
[illegible]	C1-C3	601A,	5
[4]	C4-C7	KS-21901 L1,	0.1
[2]	C8,C9	601A,	5
[3]	C10-C12	KS-21901 L1,	0.1
[3]	C13-C15	601A,	5.
[3]	C16-C18	KS-21901 L1,	0.1
[4]	C19-C22	601A,	5
[48]	C23-C70	KS-21901 L1,	0.1
[4]	C71-C74	601A,	5

RESISTOR

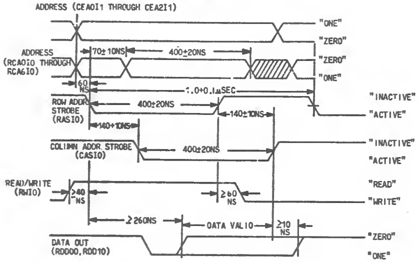
	DESIG	CODE
	R1	KS-20616 L1A, 2.15KΩ
[2]	R2,R3	KS-20616 L1A, 3KΩ
	R4	KS-20616 L1A, 2.15KΩ
	R5	KS-20616 L1A, 10KΩ
	R6	KS-20616 L1A, 1KΩ
[2]	R7,R8	KS-20616 L1A, 20.5KΩ
[4]	R9-R12	KS-20616 L1A, 14.7KΩ
	R13	KS-20615 L1A, 19KΩ

JL16 CIRCUIT PACK	DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS - JL16	SHEET 4

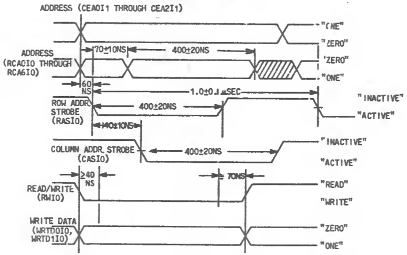
PART OF CPS JL16

CIRCUIT DESCRIPTION/TIMING

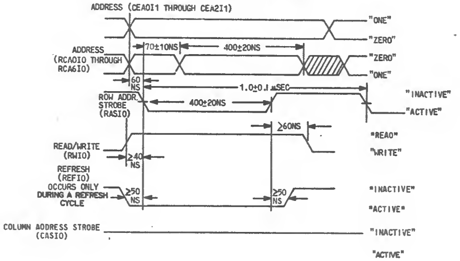
JL16 READ TIMING EXAMPLE



JL16 WRITE TIMING EXAMPLE



JL16 REFRESH TIMING EXAMPLE



CIRCUIT DESCRIPTION

THE JL16 MEMORY PLANE CONTAINS RANDOM-ACCESS STORAGE ELEMENTS MADE UP OF 16K BY 1 BIT (K = 1024) INSULATED GATE FIELD EFFECT TRANSISTOR (IGFET) DUAL IN-LINE PACKAGES (DIPS) ARRANGED IN A 128K BY 2-BIT ARRAY. THE MEMORY IS VOLATILE, IN THAT THE STORED INFORMATION WILL BE LOST IF POWER IS INTERRUPTED, AND DYNAMIC, IN THAT THE STORED INFORMATION MUST BE REGENERATED (REFRESHED) AT SPECIFIED INTERVALS. IN ADDITION TO STORAGE ELEMENTS, THE MEMORY PLANE CONTAINS ADDRESS AND DATA BUFFERS, CONTROL LOGIC, DEVICE SELECT DECODERS. ALL INPUTS AND OUTPUTS ARE +5 V TTL COMPATIBLE.

ADDRESS BITS CEA0I1 THROUGH CEA2I1 ARE GATED BY ONE OF THE TIMING SIGNALS RASIO AND ARE USED TO SELECT 2-OF-16 MEMORY DIPS. THE 16K RAM REQUIRES 14 ADDRESS BITS WHICH ARE MULTIPLEXED TO THE MEMORY PLANE ON INPUTS GRCA00 THROUGH GRCA60. THESE SIGNALS ARE BUFFERED AND CONNECTED TO ALL MEMORY DIPS. A SECOND TIMING SIGNAL, CASIO, IS NECESSARY TO ACHIEVE PROPER OPERATION. THIS SIGNAL IS BUFFERED INTO TWO BRANCHES WHICH EACH DRIVE EIGHT DEVICES IN THE MEMORY ARRAY.

THE MEMORY PLANE IS PUT INTO THE "WRITE MODE" BY FORCING A LOW LEVEL ON RWIO. DATA IS WRITTEN FROM INPUTS WRTDOIO AND WRT01IO DURING THE TIME WHEN BOTH RASIO AND CASIO ARE LOW.

DATA IS READ FROM THE MEMORY DEVICES WHEN RWIO IS HIGH AND BOTH RASIO AND CASIO ARE LOW. DATA IS THEN GATED TO OUTPUTS RD000 AND RD010. THE DATA OUT TRANSITIONS ARE SHOWN IN THE READ TIMING EXAMPLE, CASIO STAYS HIGH DURING REFRESH CYCLES.

EACH STORAGE CELL ON THE MEMORY PLANE MUST BE REFRESHED AT LEAST ONCE EVERY 4.4 ms, OR ELSE THE STORED CHARGE WILL LEAK OFF CAUSING THE DATA TO BE LOST. THIS REFRESH OPERATION CAN BE ACCOMPLISHED BY ENABLING THE RASIO INPUT IN THE SAME MANNER THAT IT IS PERFORMED DURING A READ CYCLE WHILE THE CASIO INPUT IS INHIBITED. THIS MUST BE PERFORMED FOR EACH OF THE 128 ROWS OF EACH OF THE MEMORY DIPS AT LEAST ONCE EVERY 4.4 ms. THE REFRESH OPERATION FOR THIS MEMORY PLANE CAN BE PERFORMED IN 128 CYCLES BY FORCING REFIO TO THE LOW STATE AND EXECUTING A CYCLE THAT ENABLES RASIO BUT INHIBITS CASIO AT EACH OF THE 128 STATES OF ADDRESS INPUTS RCA0I0 THROUGH RCA6I0 AT LEAST ONCE EVERY 4.4 ms.

JL16 CIRCUIT PACK	DWG SIZE 6S	ISSUE 1
BELL LABORATORIES	CPS-JL16	SHEET 5